Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

M.E DEGREE END SEMESTER THEORY EXAMINATIONS, APRIL-MAY 2025

Second Semester

Applied Electronics

AP4003/PAPE2408- VLSI Design Techniques

Regulations -2021/2024

Duration : 3 Hrs ***Maximum : 100 Marks***

PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)

Q.No	*Questions*	*BLT*	*CO*	*Marks*
1.	How do you calculate gate capacitance of a MOSFET?	L1	1	2
2.	Mention the Non-ideal I-V effects of MOS transistor.	L1	1	2
3.	Recall the expression for Elmore delay and state the various parameters associated with it.	L1	2	2
4.	List different types of procedural assignments in Verilog.	L1	2	2
5.	What are Klass semi dynamic flip flops and differential flops.	L1	3	2
6.	Define max-min delay constraints in sequential circuits.	L1	3	2
7.	Distinguish functionality test and manufacturing test.	L2	4	2
8.	List any two faults that occur during manufacturing.	L1	4	2
9.	Recall the operator which have highest and lowest precedence.	L1	5	2
10.	Blocking and non-blocking statements differ in execution. Explain how?	L1	5	2

PART – B (ANSWER ALL QUESTIONS) (Marks 5*16 = 80)

Q.No			*Questions*	*BLT*	*CO*	*Marks*
11.	a	i	Describe the equation for source to drain current in the three regions of operation of a MOS transistor.	L3	1	8
		ii	An nMOS transistor has the following parameters: • gate oxide thickness= 10nm, • relative permittivity of gate oxide=3.9, • electron mobility= 520 cm^2/V-sec, • threshold voltage= 0.7 V, • permittivity of free space= 8.85 x 10^{-14} F/cm and • (W/L) =8. Calculate the drain current when (V_{GS} = 2V and V_{DS} =1.2 V) and also compute the gate oxide capacitance per unit area. Note that W and L refer to the width and length of the channel respectively.	L3	1	8

			Or			
	b	i	Explain in detail about Layout design rules and also design a symbolic diagram and stick diagram for 2 input NAND gate.	L3	1	8
		ii	Explain in detail about Long-Channel I-V Characteristics of MOS transistor.	L3	1	8
12.	a	i	Explain path logical effort, path electrical effort, path effort and branching effort.	L3	2	8
		ii	Discuss in detail the various power dissipation components in a circuit and methods to minimize them.	L4	2	8
			Or			
	b	i	Develop a Verilog HDL code for an 8-bit shift register.	L4	2	8
		ii	Discuss the role of SPICE simulations in circuit design and analyze different device models used.	L3	2	8
13.	a	i	Explain various circuit pitfalls and their impact on digital circuit performance.	L2	3	8
		ii	Design a timing-optimized sequential circuit that incorporates time borrowing.	L4	3	8
			Or			
	b	i	Explain the impact of clock skew on circuit performance and discuss mitigation techniques.	L4	3	8
		ii	Explain metastability in sequential circuits and discuss at least one method to minimize its impact.	L2	3	8
14.	a	i	Explain the principles of silicon debugging and the challenges involved.	L2	4	10
		ii	Compare and contrast different text fixtures used in CMOS testing.	L4	4	6
			Or			
	b	i	Explain various Design-For-Testability (DFT) techniques and their role in VLSI testing.	L2	4	10
		ii	Compare boundary scan testing with traditional in-circuit testing methods.	L4	4	6
15.	a	i	Describe the 3 ways of specifying delays in continuous assignment statements.	L3	5	8
		ii	Draw the three input CMOS NOR and NAND gates and write the Verilog switch level modeling for both.	L3	5	8
			Or			
	b	i	Draw an active high 2/4 decoder using NOR gates and write the Verilog gate level description.	L3	5	8

ii	Explain the different timing controls available in Verilog HDL.	L3	5	8